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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/721,999	11/26/2003	Naoya Watanabe	67161-111	6533

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McDermott, Will & Emery
600 13th Street, N.W.
Washington, DC 20005-3096

EXAMINER	
YOHA, CONNIE C	
ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 06/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/721,999	WATANABE, NAOYA
	Examiner	Art Unit
	Connie C. Yoha	2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Connie C. Yoha

CONNIE C. YOHA
PRIMARY EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/26/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office acknowledges receipt of the following items from the Applicant:

Papers submitted under 35 U.S.C. 119(a)-(d) have been placed of record in the file.

Information Disclosure Statement (IDS) filed on 11/26/03 was considered.

2. Claims 1-7 are presented for examination.

Claim Objections

3. Claim 1 is objected to because the limitation defining the variable N and M are defined prior to the variable being used causing confusion. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper form.

Claim Rejections - 35 USC ∋ 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1-7 are rejected under 35 U.S.C. 102(e) as being anticipated by Watanabe et al, Pat. No. 6888776 (cited IDS).

With regard to claim 1, Watanable discloses a memory device comprising a plurality of memory banks (fig. 79, BA#1, BA#0) each having rows that can be activated independently of another memory bank (col. 1, line 57-60), wherein where N is a natural number equal to or greater than two and M is a natural number equal to or greater than

two and equal to or smaller than N-1 (fig. 79), a first memory bank (fig. 79, BA#) of said plurality of memory banks includes first to N-th sub-memory blocks (fig. 79, SMA0-SMA3), an M-th sub-memory block (fig. 80, MB0-MB7) of said first to N-th sub-memory blocks includes a first memory cell array (fig. 34, MB0) including a plurality of memory cells arranged in rows and columns (col. 48, line 59-61) and a first local control circuit (fig. 35, LOCT0-11), in a refresh mode, starting an operation of successively selecting rows of said first memory cell array in response to a first refresh end signal received from an (M-1)th sub-memory block and instructing a refresh start to an (M+1)th sub-memory block when said operation of successively selecting rows ends (col. 11, line 27-35) (col. 51, line 47-63), and said first memory bank further includes a plurality of sense amplifier bands (fig. 80, SAB0) each shared by adjacent two of said first to N-th sub memory blocks (col. 2, line 7-16).

With regard to claim 2, Watanable discloses wherein each of said first to N-the sub-memory blocks (fig. 34, SMA) includes a plurality of word lines for performing row selection for a memory cell (fig. 34, WL), said semiconductor memory device further comprising: an address counter (fig. 34, 204) generating a refresh address for use in common in said first to N-th sub-memory blocks to select one of said plurality of word lines (col. 51, line 5-60); and an address bus (fig. 34, 206) transmitting said refresh address to said first to N-th sub-memory blocks.

With regard to claim 3 Watanable discloses wherein said M-th sub-memory block (fig. 34, MB0-MB11) includes first to K-th word lines (fig. 34, WL<511:0>) for performing row selection for a memory cell, where K is a natural number equal to or

greater than two, and said first local control circuit (fig. 35, LOCTO) includes a row address decoder (fig. 35, 240) activated in response to the first refresh end signal received from the (M-1) sub-memory block for decoding a refresh address to select one of said first to K-th word lines (col. 51, line 24-46) and refresh end diction circuit outputting a second refresh end signal to instruct a refresh start to said (M+1)th sub-memory block when said refresh address corresponds to a refresh end of said K-th word line (col. 11, line 27-35) (col. 51, line 47-63).

With regard to claim 4, Watanable discloses wherein said first sub-memory block includes a second memory cell (fig. 34, MB1) including a plurality of memory cells arranged in rows and column and a second local control circuit (fig. 35, LOCT1), in a refresh mode, starting an operation of successively selecting rows of said second memory cell array in response to a third refresh end signal received from the N-th sub-memory block and instructing a refresh start to a second sub-mmeory block when said operation of successively selecting rows of said second memory cell array ends (col. 11, line 27-35) (col. 50, line 12-42).

With regard to claim 5, Watanable discloses wherein said first local control circuit includes first refresh start control circuit inativated in response to a reset signal and activated in response to said first refresh end signal received from said (M-1)th sub-memory block for outputting a first refresh start signal (col. 50, line 12-42), and said second local control circuit includes a second refresh start control circuit activated in response to said reset signal and activated in response to said third refresh end signal

received from said N-th sub-mmeory block for outputting a second refresh start signal (col. 63, line 11-column 64, line 35) (col. 72, line 57-67).

With regard to claim 6, Watanable discloses memory device comprising a first memory block (fig. 79, BA#1) wherein said first memory block includes a plurality of sub-memory blocks (fig. 79, SMA0-SMA1) being refreshed in a circulating manner in a refresh mode (col. 11, line 27-35), each of plurality of sub-memory blocks (fig. 34, SMA) includes a memory cell array (fig. 34, MB0-MB11) including a plurality of memory cells (fig. 35, MC) arranged in rows and columns and a local control circuit (fig. 35, LOCT11) performing an operation of successively selecting rows of said memory cell array in response to an end of a refresh operation in a sub-mmeory block at a previous stage which precedes by one in refresh-circulating order of said plurality of sub-memory blocks (col. 11, line 27-35) (col. 51, line 47-63), and refresh cycle period in each of said plurality of memory blocks is determined depending on a number of said sub-memory blocks included in said first memory block (col. 72, line 27-36) (also with regard to claim 7).

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicants' disclosure. Hidaka (6538953), Khang et al (6111808) and Aichelmann, Jr. et al (4172282) disclosed a memory device comprising plurality of blocks and banks having refresh operation.

6. When responding to the office action, Applicants= are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

7. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02 (b)).

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to whose telephone number is (571) 272-1799. The examiner can normally be reached on Mon. - Fri. from 8:00 A.M. to 5:30 PM. The examiner's supervisor, David Nelms, can be reached at (571) 272-1787. The fax phone number for this Group is (703) 872-9306. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-0956.

9. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov should you have questions on access to the Private Pair system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

C. Yoha

June 2003

CONNIE C. YOHA
PRIMARY EXAMINER